

Spread Spectrum Clock Generator

Background of the Invention

5 The subject application is directed generally to the art of synchronous digital circuitry, and more particularly to synchronous digital circuitry in which a lessened effect of electromagnetic interference ("EMI") is desirable.

 Most digital devices today operate synchronously. That is, data processing operations occur under a timing dictated by a digital clock signal. Such digital clock
10 signals are typically square waves that oscillate at a selected frequency. As improvements are made to digital processing devices, clock frequencies may be increased. Faster clock frequencies allow for improved data processing throughput. Current digital clock frequencies are already in the multi-gigahertz range. As clock frequencies continue to rise, an increased incidence of electromagnetic interference
15 exists. Such EMI requires that special shielding or casing be developed to dampen such interference. EMI can cause data errors in associated data processing devices, as well as provide for radio frequency ("RF") interference for analog devices such as radios and televisions.

 Designers have become aware that implementing a spread spectrum clock
20 generator ("SSCG") works to substantially reduce the high energy spikes associated with digitally-generated EMI.

 SSCG circuitry functions to vary slightly a frequency of a digital clock signal over time. This is accomplished by reducing "noise" associated with harmonics of a large scale integration ("LSI") clock signal. SSCG circuitry functions to alter slightly a
25 signal interval and thus diffuses a frequency spectrum and lowers a peak value.

 A side effect from the use of an SSCG is an introduction of a slight jitter in the system clock. However, such jitter is generally of little consequence other than in particular applications relating to communication network interfaces or input/output interfaces, as well as other applications having varying tolerance to jitter. Thus, it is
30 desirable to be able to vary a degree of frequency shift and associated jitter to accommodate a lessening of peak EMI while simultaneously minimizing the jitter to acceptable application parameters.

Current SSCG circuitry employs frequency comparators and voltage controlled oscillators ("VCO") to accomplish the shifting of frequency to result in a modulated clock signal. While effective, such analog-based implementations render it difficult and expensive to accomplish an SSCG circuitry, particularly in applications when a system is
5 desired to coexist on other standard digital circuitry and in conjunction with a single substrate.

The subject invention provides for a digital spread spectrum clock generator which accomplishes selected frequency variation of an associated digital clock while minimizing the required use of extensive or incompatible analog circuitry.

10

Summary of the Invention

In accordance with the subject invention, there is provided a spread spectrum clock generator which includes a divider for lowering a frequency of an input clock signal. A digital counter is incremented synchronously with the clock signal. The
15 counter, in turn, processes through a selected sequence of outputs to be generated by a pattern generator. The pattern generator output, in turn, is communicated to a digitally controllable delay circuit into which the lowered frequency clock signal is provided. Thus, a variation in frequency to the clock signal is controlled by the selected pattern in the pattern generator. This varying frequency clock signal is then multiplied to a higher
20 overall frequency compatible with the original clock signal, and output as a clock signal to remaining, synchronous digital circuitry.

In accordance with another aspect of the present invention, the frequency variation of the modified clock signal is toggled between a selected higher limit and selected lower limit.

25 In accordance with another aspect of the present invention, a method is provided for generating a spread spectrum clock signal in accordance with the foregoing.

Summary of the Drawings

The subject invention is described with reference to certain parts, and
30 arrangements to parts, which are evidenced in conjunction with the associated drawings which form a part hereof and not for the purposes of limiting the same in which:

Fig. 1 is a schematic of a conventional spread spectrum clock generator;

Fig. 2 is a diagram of the improved spread spectrum clock generator of the present invention;

Fig. 3 is a block diagram of the spread spectrum clock generator of the subject invention inclusive of a master clock, the frequency of which is lowered prior to alteration of a frequency and raised after completion thereof;

Fig. 4 is a diagram of the input clock wave form as compared to the output clock which has been processed for spread spectrum frequency modulation; and

Fig. 5 is a graph of clock period versus frequency delta associated with the spread spectrum clock generation of the subject invention.

Detailed Description of the Preferred Embodiment

Turning now to the drawings wherein the illustrations are for the purpose of illustrating the preferred embodiment only, and not for the purpose of delivering the same, Fig. 1A shows a block diagram of a conventional spread spectrum clock generator. In a conventional system, a clock input 10 was provided as one input to a frequency phase comparator 12. An output of the comparator 12 was provided to a charge pump 14, the output of which is provided to a voltage controlled oscillator ("VCO 16"). Output 18 of the VCO 16 forms a system clock output, as well as a feedback loop into frequency comparator 12 via a 1/N divider 20.

A conventional spread spectrum clock generator employed an RC circuit 22 as a filter to ground. A signal generator 24 served to generate a waveform (such as that evidenced in Fig. 1B) into the input of the VCO 16. By injecting this signal into the VCO input, an output frequency at output 18 was modulated in conjunction with the waveform of Fig. 1B.

It will be appreciated by the view of Figs. 1A and 1B that the basic circuitry employed in the spread spectrum clock generator was that of a phaselock loop. The system, while functional, relied heavily on analog circuitry and was thus not readily adaptable to implementation in conjunction with digital circuitry.

Turning now to Fig. 2, the basic architecture of the spread spectrum clock generator of the present invention is described. The SSCG A includes a clock input 30, which input is provided by the standard clock generated in conjunction with a frequency associated with an associated synchronous digital system. The clock input from 30 is
5 communicated to an input 32 of a digital delay line 34. The input 30 is also communicated to an input 36 of a counter 38. The counter 38 is suitably comprised of any simple binary counter. In the preferred embodiment, the counter 38 functions to count an increment on the basis of a number of input clock signals generated at counter input 36.

10 The counter 38 is in data communication with the pattern generator 40 through its output lines thereof (not shown). In a simple binary counter, a series of binary lines are provided which correspond to a base numeric sequence. In a preferred embodiment, a particular binary number placed on an input to the pattern generator results in the providing of a preselected digital value at an output 50 thereof. A particular pattern of a
15 pattern generator 40 of the preferred embodiment will be detailed in conjunction with Table 1, below. In the preferred embodiment, sequencing the counter 38 will result in a periodically repeating pattern being generated by pattern generator 4 at output 50.

Table 1 The TRUTH table of Pattern Generator

[illegible]

5

is suitably fabricated from digital elements and avoids implementation of the VCO/PLL circuitry as provided in connection with Fig. 1A, above.

Turning now to Fig. 3, the SSCG A of Fig. 1A is shown in connection with additional support circuitry. Conventional switching circuitry currently operates in the multi-gigahertz range. It will be appreciated that implementation of the counter, pattern generator and digital delay line, such as described herein, is more readily adapted to perform at lower frequencies than this. The additional structure of Fig. 3 accomplishes the beneficial advantages of the subject invention while facilitating use in connection with substantially higher clock frequencies. An input from a master clock 60 has communicated to a divider 62 to divide the frequency thereof. In the preferred embodiments, divider 62 is a 1/3 divider. By way of example, an input master clock frequency of 48 MHz provided at input 60 would result in a 16MHz signal being provided at the output of divider 62, which forms the clock input 30. Thus, a period of 20.83 microseconds can be extended to a period of 62.5 microseconds. The function of the SSCG A is as described in connection with Fig. 2, above.

Turning now to the output 52 of digital delay line 34 in Fig. 3, in this embodiment the output forms an input to a phaselock loop 70. As will be appreciated by one of ordinary skill in the art, the PLL 70 suitably serves as a signal conditioner to clean an output pulse, as well as a system for stepping up an input frequency. The PLL 70 suitably takes an input of 16 MHz, as provided from the output 52 of the digital delay line 34, and outputs a substantially higher frequency, 400 MHz in the preferred embodiment and which output is provided at 72. Also, an internal divider 74 suitably provides feedback at terminal 76 to allow for the enhanced output at 72.

Turning now to Fig. 4, a comparison of an input clock and an output clock 82 is described as a function of time. The input clock shows a suitable system clock input, such as may be provided at digital delay line input 30 (Fig. 1A) or master clock input 60 (Fig. 2). An output waveform 82 evidences a skew in frequency as provided by the SSCG circuitry described above.

Turning now to Table 1, disclosed is a suitable true table of the content of a pattern generator such as described herein. In the preferred embodiment, the decoder content of the subject invention will be applied with every 564 clock cycles. In this

fashion, a modulation frequency of around 28 KHz is provided. As used in Table 1, S refers to "step", D "delay value", and V refers to "decoder value". The step value S is incremented with every input clock pulse, such as that provided at input 30 (Fig. 1A or Fig. 2). A specified delay value and decoder value follows every increment of the counter 38. While the values of Fig 1A are provided in the preferred embodiment, it will be appreciated that other suitable values may be implemented to accomplish the delays of the subject invention.

Turning now to Table 2, an exemplary output of the pattern generator 40 is detailed. As evidenced in Table 2, the counter will increment at every input clock. At such point as a counter shows a value of 16, the next value will be reset to a 0. Thus, the pattern generator will decode a counter value to appear in the column "Pattern" and feed it to the delay line (50) (Figs. 2 and 3). As noted above, the delay line 34 will delay an input clock by the value given from its input 50. By way of example, when a counter value is set at 0, delay value is 0. When a counter achieves 1, the delay is 1. Next, the delay value will skip 1 and the result will be 3. As evidenced in Fig. 2, the values of column DELTA P show the difference between each adjacent account. This sequence of delta values, up and down in the preferred embodiment, is evidenced therein.

Table 2 Example of pattern generator table

| Count | Pattern | DELTA T | Delta T |
|-------|---------|---------|---------|
| 0 | 0 | 0 | 0.00% |
| 1 | 1 | 1 | 0.05% |
| 2 | 3 | 2 | 0.10% |
| 3 | 6 | 3 | 0.15% |
| 4 | 10 | 4 | 0.20% |
| 5 | 13 | 3 | 0.15% |
| 6 | 15 | 2 | 0.10% |
| 7 | 16 | 1 | 0.05% |
| 8 | 18 | 0 | 0.00% |
| 9 | 16 | -1 | -0.05% |
| 10 | 13 | -2 | -0.10% |
| 11 | 10 | -3 | -0.15% |
| 12 | 6 | -4 | -0.20% |
| 13 | 3 | -3 | -0.15% |
| 14 | 1 | -2 | -0.10% |
| 15 | 0 | -1 | -0.05% |

Referring back to Fig. 3, when an input to the SSCG A is at a value T, a first period and its corresponding output is T1-T0, which is T+ Δ . As used herein, Δ is a unidelay of the delay line. As used herein:

5

$$\begin{aligned}T1-T0 &= T + \Delta \\T2-T1 &= T + 2 * \Delta \\T3-T2 &= T + 3 * \Delta \\T4-T3 &= T + 4 * \Delta \\T5-T4 &= T + 3 * \Delta\end{aligned}$$

Turning now to Fig. 5, discloses a graph evidencing the frequency modulation scheme of the preferred embodiment. With the implementation described in the preferred embodiment, detailed above, it will be appreciated that the frequency modulation scheme employed by the circuitry of the subject invention provides for modulation analogous to that provided in conventional circuitry, as evidenced by Fig. 1B. Thus, the subject system provides for spread spectrum clock generation so as to provide all the advantages of the earlier system, but in a substantially improved, digital structure that is readily adaptable to integration and low cost and effective applications.

The foregoing description of a preferred embodiment of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Obvious modifications or variations are possible in light of the above teachings. The embodiment was chosen and described to provide the best illustration of the principles of the invention and its practical application to thereby enable one of the ordinary skilled in the art to utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. All such modifications and variations are within the scope of the invention as determined by the appended claims when interpreted in accordance to the breadth to which they are fairly, legally and equitably entitled.